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November 15, 2007

Facsimile transmitted to: 571-270-9945
Total Transmission: 6 pages

Attention: Michelle Williams

Re:

Applicant :	Mark Suska
Serial No.:	09/742,723
Patent No.:	6,972,790
Filed:	December 6, 2005
Docket No.:	GOWL-33214

Dear Ms. Williams:

Enclosed please find a copy of the letter which was faxed on June 25, 2007 in this case. Please contact me if you have any questions. Thank you very much for your help in this matter.

Very truly yours,

Lisa Pittman
Secretary to John P. Murtaugh

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June 25, 2007
Via Fax 1-571-273-8300
Total Transmission – 1 Page

Attn: The Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: **THIRD REQUEST FOR CERTIFICATE OF CORRECTION**

U.S. Patent No.	6,972,790 B2
Issued:	December 6, 2005
Title:	HOST INTERFACE FOR IMAGING ARRAYS
Inventors:	Mark Suska
Our Docket:	33214

Sir:

On June 6, 2006, the undersigned attorney of record for the above-referenced patent application mailed the following documents to the U.S. Patent Office:

1. Letter Requesting Second Certificate of Correction
2. Incorrect Certificate of Correction issued May 30, 2006
3. Proposed Second Certificate of Correction
3. Supporting Documentation

A recent check of the U.S. PTO's PAIR system for the above-referenced patent showed that the U.S. Patent Office received these documents on June 9, 2006, and copies of these documents are saved in the Image File Wrapper in the PAIR system. To date, applicant's undersigned attorney has not received the requested Second Certificate of Correction or any correspondence from the U.S. PTO relating thereto. It is requested that the Second Certificate of Correction requested in our June 6, 2006 mailing which was received by the U.S. PTO on June 9, 2006 be completed and mailed at an early date to the undersigned attorney of record.

Respectfully submitted,

By _____
John P. Murtaugh, Reg. No. 34226

JPM/li

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office at 1-571-273-8300 on the date indicated below.

John P. Murtaugh
Name of Attorney for Applicant(s)

6-25-07
Date

_____
Signature of Attorney

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June 6, 2006

Attn: The Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: U.S. Patent No.: 6,972,790 B2
Issued: December 6, 2005
Title: HOST INTERFACE FOR IMAGING ARRAYS
Inventor: Mark Suska
Our Docket No.: 33214

Sir:

This is a second request for a Certificate of Correction under 35 U.S.C. 254 to correct Patent Office printing errors in the above-identified patent. The first request was sent March 22, 2006. Enclosed herewith is the original Certificate of Correction dated May 30, 2006. The certificate should state either "Column 10, Claim 19, Line 2" or "Column 10, Line 13". Also enclosed is the proposed Certificate of Correction (Form No. PTO-1050) and documentation in support of the proposed corrections for consideration which were sent with the first request.

It is requested that a new Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record.

Respectfully submitted,

By John P. Murtaugh
John P. Murtaugh, Reg. No. 34226

JPM/ck
Enclosures: Form PTO/SB/44

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

John P. Murtaugh
Name of Attorney for Applicant(s)

6-6-06 John P. Murtaugh
Date Signature of Attorney

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,972,790 B2
DATED : December 6, 2005
INVENTOR(S) : Mark Suska

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10,
Line 2, after "claim", delete "16" and insert -- 15 --.

Signed and Sealed this

Thirtieth Day of May, 2006

JON W. DUDAS
Director of the United States Patent and Trademark Office

PTO/SB/44 (07-03)
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,972,790 B2
DATED : December 6, 2005
INVENTOR(S) : Mark Suska

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 19

Line 2, after "claim", please delete "16" and insert therefor –15–.

MAILING ADDRESS OF SENDER: John P. Murtaugh
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PATENT NO. 6,972,790 B2

No. of additional copies
⇨ 0

Amendment filed 5/24/05

Re-numbered claim 15

16. (Currently amended) An integrated semiconductor imaging circuit ~~as claimed in claim 15 where the interface includes~~ for use with an electronic processing system having a data bus comprising:

- an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and
- an interface integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system, the interface including:
  - a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor; and
  - a circuit for controlling the transfer of the data from the memory to the data bus at a rate determined by the electronic processing system.

17. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes a first-in first-out (FIFO) buffer.

18. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.

19. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

Re-numbered claim 19

20. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes an addressable memory.

a configuration register storing configuration data for the addressable memory;

a read control for controlling the read-out of the addressable memory; and

a bus command unit for receiving control of the system bus and providing an address for the data read-out from the addressable memory.

14. An interface as claimed in claim **13** wherein the interface further includes an array register for determining the dimension of the imaging array data.

15. An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:

an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and

an interface integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system, the interface including:

a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor; and

a circuit for controlling the transfer of the data from the memory to the data bus at a rate determined by the electronic processing system.

16. An integrated semiconductor imaging circuit as claimed in claim **15** wherein the memory includes a first-in first-out (FIFO) buffer.

17. An integrated semiconductor imaging circuit as claimed in claim **16** which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.

18. An integrated semiconductor imaging circuit as claimed in claim **16** which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

19. An integrated semiconductor imaging circuit as claimed in claim **16** wherein the memory includes an addressable memory.

20. An integrated semiconductor imaging circuit as claimed in claim **19** which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.

21. An integrated semiconductor imaging circuit as claimed in claim **19** which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

* * * * *